

D3.3

REPORT ON IMPLEMENTATION OF OPTIONS FOR MONITORING OF WORKPIECE AND MACHINES

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D3.3 Report on implementation of options for monitoring of workpiece and machines

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Short abstract:	This deliverable contains a detailed description of the implemented sensor and monitoring systems in 5G-SMART for the Aachen trial site. This includes descriptions of hardware developments such as sensor probes, sensor electronics, and mechanical design. Furthermore, the architecture of the implemented embedded software for operating the sensor solutions is described. Additionally, the document contains information about the used connectivity and synchronization solutions. For the sensor data processing pipeline, a factory cloud system has been set up with a tailored 5G Non-Public Network (NPN) integration concept and software services.
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Executive summary

This document reports on the implementation of the system solutions for monitoring manufacturing processes and machines in the context of the 5G-SMART project and its trial site in Aachen.

Two different sensor solutions are explained, which have different performance requirements leading to different system concepts. For both sensor systems, dedicated hardware and software concepts have been developed. This document describes the implemented hardware design concepts, including the used sensor probes, custom-built sensor electronics, interfaces, and mechanical integration concepts. A part of each sensor system is the 5G communication module and a novel synchronization solution, which generates timestamps with very high accuracy.

The two sensor solutions contain embedded processing systems such as FPGAs or microcontrollers for the operation of the sensor systems, signal processing, and generation of data packets. The document also describes the architecture of the developed embedded software.

For sensor data processing, a factory cloud system has been set up to provide a flexible and scalable processing pipeline for sensor data transmitted by the 5G sensor systems. The description of the pipeline focuses on the overall setup of the OpenStack/Kubernetes-based platform, reliability features and routing rules, and the overall integration concept. An integration concept with multiple security zones described in the document allows for flexible routing of data from the 5G system through virtual machines to the shopfloor network. Processing happens in different microservices and virtual machines, before data is fed back to the machines. The security zones have different access levels to allow flexible access to virtual machines, even for users outside the Fraunhofer IPT network at the project's trial site in Aachen.

The implemented solutions are designed according to the use case requirements described in 5G-SMART's deliverable D1.1 and based on the design options from deliverable D3.2. Both sensors and the data processing pipeline will be used to validate the use cases in relevant manufacturing tasks reflecting real-world problems in today's production.



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List of abbreviations

ADC	Analog to Digital Converter
AE	Acoustic Emission
CPU	Central Processing Unit
DHCP	Dynamic Host Configuration Protocol
DMA	Direct Memory Access
DSP	Digital Signal Processor
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Arrays
GEC	German Edge Cloud
GEM	Genior Modular
GEM-VM	Genior Modular Virtual Machine
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
12C	Inter-Integrated Circuit
IEPE	Integrated Electronics Piezo Electric
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
LTE	Long Term Evolution
LwIP	Light-Weight TCP/IP
LWM2M	Light-Weight Machine-to-Machine
M2M	Machine-to-Machine
MQTT	Message Queuing Telemetry Transport
MSP	Multi-Sensor Platform
MTC	Machine Type Communication
NPN	Non-Public Network
NTP	Network Time Protocol
PCB	Printed Circuit Board
PL	Programmable logic
PPS	Pulse Per Second
PTP	Precision Time Protocol
RAN	Radio Access Network
REST	Representational State Transfer
RTOS	Real-Time Operating System
SD Card	Secure Digital Card
SDIO	Secure Digital Input Output
SoC	System-on-Chip
SPI	Serial Peripheral Interface
TDD	Time-Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UE	User Equipment



UDP	User Datagram Protocol
USB	Universal Serial Bus
UTC	Coordinated Universal Time
VM	Virtual Machine

Table 1: List of abbreviations (Product-related abbreviation in italics)



1 Introduction

The Fraunhofer IPT trial site in Aachen is one of the three trial sites within the 5G-SMART project equipped with a 5G communication infrastructure and multiple machine tools on the shopfloor of Fraunhofer IPT. Research activities in the trial site, therefore, focus on enhanced manufacturing.

To push manufacturing processes closer to the physical limits is an ambition that challenges manufacturing companies for decades. Therefore, guaranteeing flawless machining processes is often connected with monitoring the involved assets, i.e., workpieces, machines, and the surrounding environment.

5G-SMART addresses the question, how 5G can support monitoring using wireless sensor systems. Furthermore, data processing in on-premise edge-cloud systems, also called *factory cloud* in the context of 5G-SMART, and its integration with the 5G system and production IT, is of high interest to many companies. Works carried out at the Fraunhofer IPT trial site provide valuable insights into these questions.

1.1 Objective of the document

Work for the Aachen trail site of the 5G-SMART project aims at providing two different sensor solutions for manufacturing: a versatile multi-sensor platform (MSP) for monitoring manufacturing processes and condition monitoring of machine tools, and an acoustic emission (AE) sensor solution for the monitoring of the cutting tool condition. Additionally, a versatile cloud pipeline will be established for short time-to-answer processing of sensor data and efficient machine-to-machine (M2M) communication.

Concept and design options for the solutions mentioned above have been described in deliverable D3.2 [5GS20-D320], and the targeted use cases have been described in deliverable D1.1 [5GS20-D110]. The wireless infrastructure at the Aachen trial site is described in deliverable D3.1 [5GS19-D310].

This document provides detailed information on the design options chosen for implementation and hardware and software prototype development.

1.2 Structure of the document

Each of the following sections describes a specific implemented solution, starting with a brief description of the underlying use case for which the solution has been designed. Next, the sections include information about the physical principles of the different sensing probes, which help understand the chosen design options, followed by in-depth descriptions about the hardware architecture and the setup in terms of electrical design and components used in the setup. Each section contains all relevant information about the (embedded) software needed to operate and configure the different sensor solutions and generate data packets for the attached 5G communication module.



Section 2 describes the implemented wireless AE sensor system. The description of the MSP in Section 3 contains information about the 5G communication module and power supply and the hardware and software layout of the overall MSP. The section concludes with the synchronization solution implemented, especially on the MSP. Section 4 describes the sensor data processing pipeline consisting of the architecture of the factory cloud system and the implemented software architecture chosen for the processing of sensor data and feedback via M2M communication. Finally, the document ends with the main conclusions in Section 5, providing also an outlook.



2 Implementation of the wireless acoustic emission sensor system

The term acoustic emission (AE) refers to sound waves, which spread in a solid object. For example, in machining processes, acoustic emission is caused by the forces acting on tools and workpieces. It induces measurable vibrations, which allow drawing conclusions about the quality of the machining process. AE sensors are widely used for monitoring cutting processes, especially for performing the following tasks:

- Monitoring of tool wear
- Detection of tool breakage
- Detection of collision of the machine spindle
- Detection of inhomogeneities in the workpiece material

In addition to normal stresses, a solid object can also absorb shear stresses, allowing transverse waves and independent longitudinal waves to propagate in solid objects. AE sensors, like the *AE-C* sensor from Marposs Monitoring Solutions (MMS), can detect these waves.

2.1 Hardware

Figure 1 shows the concept for the use case architecture including the wireless AE system. This architecture includes a machine-integrated approach with a high grade of communication efficiency to bring data from the sensor to the analysis and monitoring hardware via the 5G network with low latency. The monitoring hardware (the GEM monitoring unit in Figure 1) is connected to the machine with a reliable and safe Fieldbus system. The machine is monitored and controlled based on an AE sensor mounted on the machine table near the machined part. The electronic circuitry includes components for amplification, filtering, and sampling sensor data with high rates. The raw data and the pre-processed data can be passed through the signal processing unit to the 5G transceiver, as configured during operations.

2.1.1 AE sensor

The AE-sensor used in the 5G SMART project is the *AE-C* sensor from MMS shown in Figure 2. The sensor is industry proven and comes in an IP66/IPx7 chrome-nickel steel housing resistant to cooling lubricants. The *AE-C* sensor uses the Integrated electronics piezo electric (IEPE) interface, a standard interface for piezoelectric sensors. IEPE is an analog interface where the voltage is measured. Supplying the sensor with a constant current reduces the noise of the signal. The frequency range of this sensor is between 10 and 400 kHz.





Figure 1 High-level architecture for a 5G wireless acoustic emission sensor system



Figure 2 AE-C sensor from Marposs Monitoring Solutions

2.1.2 Signal Conditioning Module

The sensor is connected to a signal conditioning module. Figure 3 shows the structure of this signal conditioning module. On the board, 8th-order analog high-pass and low-pass filters in the form of Sallen-Key filters are used to remove aliasing effects and noise at low frequencies from the signal.



Figure 3 Structure of the signal conditioning module

The output signal is then boosted to a virtual ground point, and the level is adjusted. In addition, the signal conditioning module has two floating digital outputs. A constant current diode generates the constant current for the ICP interface. The connectors are positioned to be plugged onto the Cora Z7 board described in section 2.1.3. Figure 4 shows the signal conditioning module developed for this project.



Figure 4 Signal conditioning module

2.1.3 FPGA processing module

The conditioned analog AE signal must be digitalized and pre-processed before being sent to the cloud for analytics. Since the data sample rates are very high, and since the system should provide low latency for pre-processing in real-time applications, an FPGA-based System on Chip (SoC) design is preferred to reach the required performance. In an FPGA-based SoC, a hardwired microcontroller (ARM architecture in our case) is tightly coupled with a programming logic (FPGA logic). This architecture enables the high-performance computation modules, such as the Fast Fourier Transform (FFT) calculations, to be offloaded to the FPGA side. At the same time, the communication of data to the 5G communication module is processed by the microcontroller. Thus, this architecture increases the performance without creating a processing bottleneck. Figure 5 shows the Xilinx Zynq 7000 Series System on Chip architecture used in the AE sensor system prototype.

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Figure 5 Zynq 7000 SoC architecture [XI21]

The FPGA logic is tightly coupled with the high-performance AXI ports to have high data throughput, as shown in the architecture above. The Programmable Logic (PL), consisting of logic gates, is used to implement the processing modules such as FFT directly on the gate level, significantly increasing the processing speed (Example: FFT calculation of length 1024 is 30 microseconds). The processing core accesses the data from the modules via the AXI ports. The processor collects and prepares the data as a UDP packet to be sent via the Ethernet interface.

For the AE application, a Xilinx Zynq-7000 Series-based SoC is used. A development kit from Digillent (Cora-Z7) has been used to build the application. It has a ZynQ 7010 chipset, a Cortex A9 microcontroller, and an Artix 7 FPGA logic unit. The development kit provides the following features:

- Dual-core Cortex A9 running at 667 MHz
- Artix 7 FPGA logic with
 - 4,400 Programmable logic slices
 - o 80 DSP Slices
 - 270KB Block Ram
- 512MB DDR3 Ram
- 1Gigabit Ethernet, USB, SDIO
- On-chip ADC with 1MSPS Sampling Frequency at 12-bit resolution
- SD Card Slot for storing bitstreams





Figure 6 FPGA Cora z7 Development Kit

The application can be programmed via JTAG (Joint Test Action Group) interface or loaded from an SD card. For the AE sensor system, the bitstreams are generated from the Xilinx Vivado IDE and then copied to the SD card for faster booting.

2.1.4 5G communication module

The interface of the acoustic emission sensor platform with the 5G system operating in the timedivision duplexing (TDD) N78 3.7-3.8 GHz frequency range has been carried out using a 5G communication module. For the communication module (i.e., user equipment or UE), multiple devices like the WNC Industry Router, Quectel RM500Q, HMS Cellular Bridge and Phoenix Contact 5G Industry Router were used. All devices are based on the Qualcomm x55 modem chipset. The integration of the AE platform with the communication module has been accomplished over the Ethernet interface.

In particular, WNC Industry Router (as shown in Figure 7) has been used based on extensive over-theair performance measurements and stable performance, early availability and ease of interfacing with the sensor platform. The WNC Industry Router provides a direct multi-Gbps interface for the user data traffic from/to the acoustic emission sensor platform. The WNC Industry Router supports both, nonstandalone (EN-DC) and stand-alone mode of the 5G operation in the non-public network at Fraunhofer IPT and does not require a host platform (e.g., PC or evaluation board) for integration with the acoustic emission platform. DHCP support in the WNC Industry Router flexibly allows multiple platforms, such as the acoustic emission sensor platform and multi-sensor platform, to be integrated or swapped without needing to manage/track the fixed IP addresses. The Qualcomm x55 modem chipset used in the WNC Industry Router supports various 5G radio access network (RAN) features appropriately configured to achieve the desired latency and throughput characteristics of the AE monitoring use-case at Fraunhofer IPT.

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Figure 7 WNC Industry Router as a 5G UE used in the initial characterization of the acoustic emission monitoring use-case and 5G system performance evaluation

2.2 Software Architecture

For the FPGA, two separate software architectures needed to be developed for the application: one for the FPGA programmable logic (PL) side and one for the processing side (PS). Signal data acquisition and pre-processing for feature extraction requiring low latency and real-time performance are developed on the PL side, whereas data packing and communication are done on the PS side. With this architecture, we ensure to prevent data processing bottlenecks.

2.2.1 Implementation of signal processing

The software architecture for signal data acquisition and pre-processing is shown in Figure 8.



Figure 8 Overall AE processing architecture

Due to hard real-time requirements (<1 ms latency for data packets sampled at 1 MHz), computeintensive tasks such as FFT and ADC are developed on the PL side of the SoC. Signals from the analog

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port are digitalized first by the on-chip ADC. Since FFT processes data in fixed-sized chunks, the ADC streams are first packed into adequately sized blocks and then sent to the FFT block. FFT output is complex numbers converted to the magnitude spectrum by a combination of stream splitter and CORDIC modules, which compute the multiplication of digital streams (real and imaginary component of FFT) in parallel and send these to the PS side through the DMA block.

With the AXI stream interconnect, the FPGA logic can transfer large amounts of data without causing a memory access bottleneck. For example, the logic can transfer 100 megabytes of data running at 100 MHz. The data stream of the FPGA logic is connected to the DMA block, accessed by the microcontroller to read and write the data. The controller can read out the packets through the DMA interrupt generated for every block of the processed packet received. Then, the controller accesses the DMA buffers to read the data and prepare the data packets for transmission based on the interrupt.

2.2.2 Implementation of data package generation

The following functional blocks of the software architecture (Figure 9) are developed to send AE data packets from the controller and process them on the PL side.



Figure 9 Functional blocks of SoC

The Zynq Controller operates at 667 MHz, independently of the clock on the cores of the PL side. This asynchronous clock mode enables the controller to process faster and independently of the PL cores. Data synchronization is achieved using the AXI interconnect and its interrupts. Due to the hardwired logic of the controller and the FPGA and using AXI interconnect, it is possible to configure and manage the soft IP cores from the controller.

The controller core first sets up the peripherals (Ethernet and UART), its timers, and interrupt routine. The soft IP cores implemented on the PL side, the ADC, FFT, Packet limiter, and DMA are then set up with proper configuration. The following configuration is used for the application:

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- ADC is configured for a channel mode with a sampling frequency of 1 MHz.
- The FFT is configured for processing data of 1024 samples.
- The packet limiter for FFT is configured for 1024 samples.
- DMA is modified to receive interrupt for input data streams.

The frequency range of the *AE-C* probe is 10-400 kHz, which is covering the frequencies at which the relevant AE phenomena such as tool breakage occur. According to the Nyquist criterium, the sampling has to be at least 800 kHz. Here, 1 MHz has been chosen. A value of 1024 samples was experienced as the best compromise between spatial resolution and computational load for the FFT.

After the configuration, the application sets up the interface for network communication with the 5G module via its Ethernet port. This communication involves requesting an IP address via DHCP and then setting up the socket connection to send data to the destination. The controller uses the LwIP TCP/IP stack to process the Ethernet packets and establish the network connection. In addition, the stack provides an API for socket connection and UDP packet generation.

After successful network setup, the status LED is set and the controller waits for the interrupt from the DMA module. On interrupt, data is read from the DMA core, copied to the UDP buffer and sent to the destination port.

Since the FFT magnitude spectrum data is a double-sided spectrum band, the configuration is set to send only the single-sided spectrum as a UDP packet. The UDP packet has 1024 bytes, containing the frequency bins from 0 to 512 and its corresponding amplitude. The data is transmitted every 4-5 ms.



3 Implementation of the multi-sensor platform for monitoring of workpieces and machines

3.1 Hardware

3.1.1 Layout of the MSP

Different kinds of sensors are usually placed in stand-alone systems in today's production, not being aggregated in a single platform format. Moreover, only a few of them can be used wirelessly. For this reason, connectivity, applicability and mobility are limited.

The multi-sensor platform (MSP) implements several sensors on a single board. Furthermore, several identical copies of such a device will be integrated into multiple machines in the trial site of Fraunhofer IPT in Aachen. In this way, factory and process automation can be optimized by collecting data and monitoring many workpieces simultaneously and in real-time.

The concept of MSP is shown in Figure 10. It consists of three interconnected subsystems: a set of sensors integrated into the machine or to be attached to the workpiece; a device that receives the signal from the sensors and delivers the information to the 5G network; the factory cloud that elaborates the information, generates outputs and sends a feedback to the shopfloor.



Figure 10 Integration concept of the MSP in multiple factory application scenarios

The initial ideal architecture for the MSP was a unique compact device based on integrating all the sensors in a single unit, without the need of cables, together with the microprocessor, the 5G modem, and the power supply. Such an architecture would have been particularly suited for a product mounted on different machinery and workpieces. However, for the MSP connectivity an integrated 5G module would have been required, which is not available at the time of the MSP design. In addition, since most of the sensor probes need physical contact to the measured sample, a customized mechanical unit would be required providing the physical contact on the one hand and containing the



sensor electronics on the other hand. This would only be achievable with a dedicated hardware for a specific sensing task.

For these reasons, an architecture based on a modular approach is adopted, as shown in Figure 11. Such design consists of integrating some on-board sensors into the platform, which simultaneously provide connectivity to external sensors. Furthermore, the 5G modem is also externally connected to have the possibility to change it without modifying the MSP itself. For this purpose, an ancillary communication module is connected to the core electronics of the device.



Figure 11 Modular Architecture for the MSP Device

A disadvantage of this approach is related to the footprint of this device, which is larger than required: 100mm x 100mm instead of 50mm x 30mm, possibly limiting its installation. Nevertheless, it will bring benefits from a power supply viewpoint as far as testing will be concerned.

The requirements set for the MSP in the use case definition phase in the project start are listed below:

- Resolution of measurement of data \geq 16 bit
- Small footprint
- Robustness against harsh environmental conditions
- Intelligent battery management
- Latency between MSP and factory cloud as the two end points < 10ms
- Sensors inside the housing of the MSP and external sensor interfaces

All of these parameters are implemented into the architecture of the MSP. Figure 12 shows its block diagram.

The processing core within the MSP device consists of the typical real-time embedded system:

- The microprocessor is the core of the device, selected as a trade-off between processing performance and power consumption.
- The on-board sensors include internal environment diagnostic (humidity and circuit board temperature) and monitoring sensors (gyroscope and acceleration sensor).
- Three identical external sensor interfaces are integrated in order to measure external acceleration, temperature, and strain.
- The 5G radio interface connection is external to the unit.
- The power supply design includes a Lithium-ion battery.



- The integration of a *u-blox*[™] SARA-R5 module provides time synchronization for the information stream. The module is connected to the microprocessor.
- An externally connected ancillary communication module is adapted to perform some testing in advance with 4G-LTE and be substituted later with the selected 5G solution.





A hardware description of these components is provided in the following paragraphs.

3.1.2 Hardware components on the MSP mainboard

In this section, the hardware components on the MSP mainboard are analyzed. Figure 13 shows the top layer placement, where we can see the main component, i.e., the microprocessor.

Microprocessor

The microprocessor integrated into the module is the *STMicroelectronics™ STM32F429IH*. This module represents a trade-off between processing power and power consumption. As described in deliverable D3.2 [5GS20-D320], the initial choice was among an ultra-low-power microcontroller running at a few MHz like the ARM®-Cortex-M®, or a high-level embedded one like the ARM-Cortex-A® running at hundreds of MHz, or Digital Signal Processor, like Analog Devices Blackfin®, running at a wide range of clock frequencies.

The selected *STM32F429IH* belongs to the ARM-Cortex-M^{®®} family, which consists of a whole set of 32-bit RISC microprocessors operating at frequencies up to 180MHz. It is of the UFBGA type, equipped with 176 pins.

The selection of the microprocessor is also related to the peripherals needed for communicating with the sensors. Therefore, in section 3.1.3, a detailed analysis of the main communication peripherals used to interconnect the microprocessor with the board components will be provided.

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Figure 13 MSP layer placement

Oscillators

As shown in Figure 13, there are two external quartz oscillators connected to the microprocessor.

The X101 has a frequency of 32 kHz. It is linked to the microprocessor through the pin *PC14/OSC32_IN* and the ground through *PC15/OSC32_OUT*.

The X102 has a frequency of 25MHz. It is linked to the microprocessor through the pin *PH0/OSC_IN* and the ground through *PH1/OSC_OUT*.

There are also two secondary clock sources: LSI RC (32 kHz) and LSE crystal (32.768 kHz).

Their configuration is the following:

- System Clock (SYSCLK) = 168 MHz
- High-performance Bus (AHB) prescaler = 1
- AHB clock (HCLK) = 168 MHz
- Advanced Peripheral Bus (APB1) prescaler = 4
- High-Speed External (HSE) frequency = 25 MHz
- Phase-Locked Loop (PLL) M = 25
- PLLN =336
- PLLP = 2
- PLLQ = 7
- VDD = 3.3V

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The system clock was chosen to take advantage of the maximum performance available of the microprocessor. The secondary clock employs a PLL to precisely generate the 25 MHz required by the Ethernet transceiver.

Debug

Figure 13 shows the connector for the development and debugging of the MSP board, labeled as J100. It consists of a standard 10-pin socket organized in 2 rows of 5 pins. The microprocessor programming is done through the *ST-LINK/V2*, an in-circuit debugger for the STM8[™] and STM32[™] families.

Memory

In Figure 14, the placement of the two main memory blocks of the board is highlighted.



Figure 14 Memory layer placement

FLASH Memory

The FLASH memory, labeled I301, is the *Adesto Technologies® AT45DB*. The connection to the microprocessor is provided through the integrated SPI peripheral (SPI2). It has a maximum clock frequency of 20 MHz, a minimum supply voltage of 2.7 V, and low power dissipation.

EEPROM Memory

The EEPROM memory labeled I302 is the *Microchip® 25AA040A*. Connection to the microprocessor is provided, identical to the flash memory, through the same SPI peripheral (SPI2), which is being used in a multi-master configuration. Therefore, it has a maximum clock frequency of 10 MHz and low power consumption.



3.1.3 Sensor modules

The MSP is designed to acquire a variety of different measurement quantities depending on the specific use case. In the framework of the MSP, each sensor measurement needs to be digitalized so that its information can be readily acquired, processed, and forwarded to the ancillary communication module.

The architecture of the MSP board includes both on-board and external sensors. The supported sensors on the MSP and measurands are listed below.

- On-board sensors:
 - Accelerometer sensor, used to measure the acceleration with respect to three orthogonal axes, including Earth gravity.
 - Internal temperature and humidity sensor, used to detect overheating of the electronics or eventual liquid ingress.
 - *Gyroscope,* used to monitor the workpiece orientation to detect clamping errors leading to tool and material damages.
- External sensors:
 - Strain gauge sensor, to correlate the mechanical stress on a workpiece with the force load leading to deformations.
 - Acceleration (digital) sensor, to measure the vibration of the workpiece or the tool due to their interaction with the machine. This measurement is essential to avoid effects like vibration marks or chatter marks that affect the overall part quality, ultimately leading to a rejection of parts.
 - *Temperature (digital) sensor,* used to monitor and eventually compensate the mechanical deformation of workpiece or tools due to heating.

The MSP board hardware components related to the sensor modules are described below.

On-board sensors

The placement of on-board sensors is highlighted in Figure 15; they can measure internal quantities inside the housing of the MSP.

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Figure 15 On-board sensors placement

Accelerometer

The accelerometer sensor is the *STMicroelectronics*[™] *LIS2DH12*. It can measure accelerations from 1 Hz to 5.3 kHz. It is a three linear axis component, with a 10-bit resolution and full scale of 2g, 4g, 8g, 16g.

The power consumption is very low, below 2 μ A, and the supply voltage can be in the range of 1.7-3.6 V. Two power supply decoupling capacitors are placed close to the device to minimize measurement noise: *C300* and *C301* of 100 nF each.

There are three operating modes: high-resolution mode, normal mode, and low-power mode. The *LIS2DH12* is programmed to return to the latter state automatically (return-to-sleep condition).

The output channels are X, Y, Z, and a FIFO buffer for each of them. Thus, it provides the following modes:

- Bypass Mode: the FIFO is empty, and only the first address of each channel is used.
- FIFO Mode: the buffer is filled with the data coming from the X, Y, Z channels.
- Stream Mode: the buffer gets filled with data constantly. When the buffer is full, the oldest data gets replaced by the latest one.
- Stream-to-FIFO Mode: data is collected with a combination of both modes.
- Retrieve data from FIFO: FIFO data is read.

The acceleration data is provided through an integrated SPI peripheral (SPI1). It interacts with the microprocessor through *SINT_ACC* (PA4), *SINT_SCK* (PA5), *SINT_MISO* (PA6), *SINT_MOSI* (PB5). They are connected, respectively, to the LIS2DH12 pins *CS* (2), *SCL* (1), *SDO* (3), *SDI* (4). The SPI interface allows to perform Read-and Write operations from the device registers.

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Humidity and Temperature Sensor

The sensor for humidity and temperature measurement is a *Texas Instruments*^M *HDC2022.* It contains an ADC, a calibration memory and an I^2C interface.

This sensor has a very low power consumption. It has a default power mode, the sleep mode, with a typical current consumption of 50 nA. When a measurement is triggered, it turns to measurement mode.

There are two kinds of active operating modes: one-shot and conversion. In the first one, with an I^2C command a measurement is initiated. When completed, the device goes back to default mode. In conversion mode, the device periodically wakes up from sleep mode and performs its operations. The *HDC2022* also provides a heater used to prevent condensation.

On the bus interface this device operates as a dependent device. The connection is made through *SENS2_SCL* and *SENS2_SDA*. The device address comprises seven address bits and a direction bit that indicates the read or write operation.

The *HYG_IRQ* signal is connected to the Data ready/Interrupt (*RDY/INT*) pin, whose address is set according to the Interrupt Configuration. It is used to verify if, after the measurement conversion, the data is ready.

Gyroscope

The gyroscopic sensor is the *STMicroelectronics*^m A3G4250D. It provides a measurement of the angular rate of the board.

The power consumption is low, and to limit the acquisition noise, a power supply decoupling capacitor of 100 nF (*C307*) is placed close to the device. The supply voltage has a range of 2.4-3.6 V.

A 2nd order low-pass filter is set at pin 14 (*PLLFLT*) to realize a PLL circuit.

The *A3G4250D* provides three output channels: yaw, pitch, and roll. 16-bit data FIFO is embedded for each of them. Thus, this buffer can work in five modes:

- Bypass Mode: the FIFO is empty, and only the first address of each channel is used.
- FIFO Mode: the buffer is filled with the data coming from the yaw, pitch, and roll channels.
- Stream Mode: the buffer gets filled with data constantly. When the buffer is full, the oldest data gets replaced by the latest one.
- Retrieve data from FIFO: FIFO data is read.

The angular data rate is provided through an integrated SPI peripheral (SPI1). It is a bus slave and interacts with the microprocessor through *SINT_GYR* (PA3), *SINT_SCK* (PA5), *SINT_MISO* (PA6), *SINT_MOSI* (PB5). They are, respectively, connected to the *A3G4250D* pins *CS* (5), SPC (2), *SDI* (3), *SDO* (n 4). The SPI interface allows to perform Read and Write operations from the device registers.

External sensor interface

The placement of the interface board to external sensors is highlighted in Figure 16.



Figure 16 External sensors interface placement

The connection to the MSP board is made using two socket connectors, labelled J100 and J101, with nine pins.

The MSP modular architecture comprises all identical external interfaces with a selected standard, as shown above. In such a way, different combinations of sensors can be employed or even changed during different repetitions of a test. Moreover, all types of sensors have the same electrical and mechanical connection.

The external sensors are strain gauge, acceleration sensor, and (digital) temperature sensor.

Each sensor has its specific physical interaction with the measured target, so that the automatic enumeration and configuration can be performed by the microprocessor; the manual configuration is always possible.

The three external sensor interfaces are connected to the MSP board, as highlighted in Figure 17. Connectors are organized two by two: *J600-J601*, *J602-J603*, *J604-J605*.





Figure 17 Connection between external sensor interfaces and MSP board

The three interface boards to external sensors are all made with the same components: ADC, Regulator, EEPROM Memory, Instrumentation Amplifier, all of which are described below.

ADC

The analog-to-digital converter is an *Analog Devices*[™] *AD7124-4*. It has four differential analog inputs: *AINO, AIN1, AIN2, AIN3,* which can be positive or negative, and it includes various on-chip diagnostic functions. In addition, adjacent pins are to minimize mismatches between the channels. It can have three different power modes: high power, mid power, and low power.

The on-chip registers are accessed through the SPI interface.

Regulator

The Microchip® MIC5233YM5 is an ultra-low-power voltage linear regulator.

The input voltage can be very high, with a wide range of 2.3-36 V. The quiescent current instead is only 18 μ A. The large input capacitor *C100* of 22 μ F limits the input noise to the converter. The regulator stability and transient response are further improved with an output feedback capacitor *C101* of 22 pF and a large output capacitor.

The two external resistors R101=270 k Ω and R102=215 k Ω set the output voltage to V_{out} \approx 2.8 V.

The *EN* (pin 3) disables or enables the *MIC5233YM5*; forcing the pin high enables the output voltage while forcing the pin low sends the component to "Zero" mode, with a current consumption of 0.1 μ A.

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EEPROM Memory

The EEPROM Memory is a *Microchip® 25AA040A*. This component has low power consumption and a maximum clock of 10 MHz. It can be accessed through an integrated SPI peripheral on the *SDI* (pin 3). Read and write operations can be performed.

Instrumentation Amplifier

The Instrumentation Amplifier Analog DevicesTM AD8426 is included as a first gain stage to improve the acquisition system's sensitivity. Its analog outputs are connected to the AD7124-4 analog-todigital converter. The inputs are designed to be connected to the external sensor. The architecture is based on the 3-opamp topology. It is configured for a gain of about 12 using a 0.1% tolerance resistor R116=4.42 k Ω .

3.1.4 5G communication module

The modular architecture for the MSP device provides an external connection with an ancillary communication module, which provides wireless 5G connectivity. This choice, as described in deliverable D3.2 [5GS20-320], is due to the availability of a limited set of types of 5G devices. Therefore, the 5G connectivity module is externally connected, to potentially support any device that may become available on the market and to be flexibly connected to it without changing the MSP itself.

A disadvantage of this choice is related to the device's size, whose dimensions could limit and affect the installation in machinery. Nevertheless, this allows expanding the variability of the tests, both from the sensor's point of view and from the wireless connectivity. Moreover, it is possible to start testing the system solutions using available 4G-LTE modems and then later substitute them with a 5G capable solution.



In Figure 18, a block diagram of the ancillary communication module is sketched.

Figure 18 Ancillary communication module



The initial design included the u-bloxTM TOBY-L4 platform, a 4G-LTE Cat 6 device whose bandwidth was enough for the use cases of the Aachen trial site, especially for the wireless AE system.

The 5G module is the *Quectel™ RMU500-EK* from the *RG50xQ* series.

The connection between the microprocessor and the module includes the following three interfaces: UART (Universal Asynchronous Receiver Transmitter), typically used for control operations of the modem, USB[®] (Universal Series Bus), and Ethernet for data transmission.

These kinds of high-speed serial buses require special care since their standard connectors are not waterproof. For this reason, since the architecture option with an external ancillary module has been selected, a robust waterproof mechanical connection is required.

From an electrical point of view, both are included in the design and analyzed in the paragraphs below.

Ethernet

Figure 19 highlights the layer placement of the main components of the Ethernet interface.



Figure 19 Ethernet layer placement

Signal Transformer

The *Pulse Electronics*[®] *H1102* is a signal transformer whose typical application circuit is the 10/100 BASE-Tx, the Fast Ethernet standard that provides 100 Mbps Ethernet.

From the cable side, it is connected to the interface for the connection to the ancillary module. From the chip side, it is connected to the ethernet transceiver.



Circuit Protection

To ensure ethernet protection, in addition to the data transceiver, a protection circuit is also required. The *STMicroelectronics™ USBLC64* is used to protect the circuit from electrostatic discharges (ESD), thus preventing the device's malfunction.

D0 (pin 1), D1 (pin 3), D2 (pin 4), and D3 (pin 6) are those data lines for which protection is ensured.

The ESD behavior is optimized with the addition of C715 = 100 nF from the VCC pin to GND.

Ethernet Physical Layer Transceiver

The *Micrel Inc. KSZ8081RNB* is an Ethernet Physical-Layer transceiver. Having a single power supply of 3.3V and 32 pins available, this component transmits and receives data.

It provides the Reduced Media Independent Interface (RMII), configured to operate at 25 MHz after it is powered up or upon the hardware gets reset. The external clock source is an oscillator connected to *XIN* (pin 9) with 25MHz. *XOUT* (pin 8) is connected to the ground.

The MDC/MDIO management interface allows upper-layer devices to control the state of the *KSZ8081RNB*. The *MDIO* (pin 11) is used for the management interface of Data I/Os and requires the external resistor R715=1 K Ω . The *MDC* (pin 12) is used for the management interface of Clock Input and is synchronous concerning the *MDIO*.

The Ethernet Physical Layer Transceiver connection to the Ancillary Module – as highlighted in Figure 20 – is provided through the connector *J700*.

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Figure 20 Connection to the ancillary module

This connection is provided through a magnetic interface circuit. The physical receive or transmit signals, (RX-, RX+) and (TX-, TX+), are connected to the magnetic interface circuit using an adaptation network RC with a T-connection.

USB Interface

Figure 21 highlights the main components of the USB interface placement.

USB to UART Bridge Controller

The *Silicon Labs*[®] *CP2102N* is a USB-to-UART Bridge Controller, which integrates a second USB connection into the MSP. It is composed of a USB transceiver, an internal oscillator, a UART and a USB controller, and to manage the USB and the UART data transfer.

The device is connected to the MicroUSB – B connector *J500* through *USBDM* (pin 4) and *USBDP* (pin 5) and includes USB ESD protection diodes (*V500, V501, V502, V502*). It represents the virtual serial port on USB.



Figure 21 USB interface placement

When the internal regulator is used, and the USB is connected, the power pins require the following configuration:

- *REGIN* (pin 7) connected to the 5V of USB_EXT (Vin), with two bypass capacitors placed very close, *C502*=10 μF and *C503*=100 nF.
- *VDD* (pin 6) and *VIO* (pin 5) connected to the 3.3 V of the USB, with two bypass capacitors placed very close, *C500*=4.7 μ F and *C501*=100 nF.

The UART interface consists of transmitting and receiving data signals (*TXD* and *RXD* pins) linked to a digital isolator.

Digital Isolator

The *Texas Instruments*[™] *ISO7221C* is a digital isolator. It blocks high voltages, isolates ground, and prevents noise between the USB-to-UART bridge controller and the microprocessor. Channels are oriented in opposite directions, and input and output buffer are separated by silicon.

The device is linked to the *CONSOLE_RX* (PB7) and *CONSOLE_TX* (PB6) of the microprocessor and operates at 3.3V with *VDD2* and +VCC.

MicroUSB-B

The MicroUSB-B connector, labeled *J501*, is linked to the microprocessor through the pins *OTG_FS_DM* (PA11) and *OTG_FS_DP* (PA12). The OTG (On-The-Go) is the peripheral that allows the microprocessor to act as a host.

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Time Synchronization – SARA-R5 Module

The MSP will aggregate a large number of data sources spread all over the factory. Due to the signal processing of data, the information stream must have a well-known time correlation. Therefore, the MSP device will timestamp each of them, for which time synchronization is needed.

5G allows the provisioning of a common reference time over the wireless link to 5G devices at high precision (<1 μ s). This functionality is provided with the Release 16 version of the 5G standard and is not yet available in 5G products. As an alternative to 5G NR integration inside the device, a module from *u-blox*TM was integrated, which makes use of the LPWA features of the 5G standard, and provides time synchronization. The initial other alternative was a GNSS module, the most common source of high precision time information. However, it requires constant visibility to the sky satellites, which is not the case in most production sites.

For these reasons, the design of the MSP contains a SARA-R5 module providing the CellTime[™] feature (see [UB21] and Chapter 3.3.1). The module is connected to the microcontroller.

This device is ideal for IoT applications due to:

- Security, since it includes data-protection services, anti-cloning, and secure chip-to-chip communication.
- Wide multi-regional coverage.
- Compatibility with other *u*-blox[™] families such as TOBY.

In Figure 22, the placement of the main components of the module is highlighted.

Figure 22 SARA-R5 layer placement

Power Management

The SARA-R5 requires an external DC power supply. Due to stability requirements, three VCC pins (51, 52, 53) are connected to the *Microchip® MIC2039A*. This load switch has an ultra-low resistance and can support a maximum current of 4A.

The voltage regulators, labeled *1201*, *1202*, *1203*, *1204*, *1206*, *1207*, *1208*, constitute the Power Management Unit to which the VCCs are internally connected.

Antenna Interface

The ANT (pin 56) is the cellular antenna RV interface linked to the Antenna Coaxial Connector J200.

The ANT_DET (pin 62) is needed to detect the presence of the external antenna.

System Function

The SARA-R5 supports the AT commands, according to the 3GPP standard. *PWR_ON* and *RST* (pins 15 and 18) are needed to set the module system functioning as described below.

• Power-on:

If the module is not powered, a VCC input is applied, and the PWR_ON low level is enforced; If the module is in power-off or in deep-sleep, the PWR_ON low level is enforced;

- Power-off: AT+CPWROFF command AT+CFUN=10 command Forcing a low pulse in PWR_ON and RST
- Reset: AT+CFUN=16 command

SIM interface

The SARA-R5 is connected to an external SIM through the *Würth Elektronik*^m Micro-SIM Connector. The connection between the module and the connector, labeled *J201*, is provided through *SIM_CLK*(pin 38), *SIM_IO* (pin 39), *SIM_RST* (pin 40), *VSIM* (pin 41).

Serial Communication

UART and USB communication interfaces are provided:

- UART_DSR (pin 6), UART_DTR (pin 9), UART_RTS (pin 10), UART_CTS (pin 11), UART_TXD (pin 12), UART_RXD (pin 13) are needed to communicate with the host microprocessor.
- The USB interface is required for the device diagnostics. The connection to the MicroUSB-B is provided through the J202 connector. VBUS_DET (pin 17) enables the interface, while USB_D-/USB_D+ (pin 28 and 29) provide data transport.

GPIO

GPIO1, GPIO2, GPIO4, GPIO6 are general-purpose I/Os, needed to indicate the cellular network status.

3.1.5 Power supply

Having chosen the modular architecture with an external ancillary communication unit for the MSP design, the same connector of the ancillary module also routes the power to the recharging circuit.

The Power Supply of the MSP is based on a Lithium-ion battery. This battery is a secondary battery. Therefore it must be recharged, and a recharging circuit is needed. The initial option was to use a primary battery, thus disposable, but that would have required a waterproof opening with a mechanical design for safe operation. The main components of this rechargeable circuit are highlighted in Figure 23: Battery Gas Gauge, Battery Charge, and Voltage Level Translator.

Figure 23 Power supply layer placement

Battery Gas Gauge

The electronic component for measuring the battery charge state, voltage, and chip temperature is *Linear Technology*[®] *LTC2942*.

The two main elements of this device are a coulomb counter and a voltage monitor, but an internal temperature reading is also available.

The coulomb counter determines the state of charge of the battery. To do so, it monitors the differential voltage between $SENSE^+$ and $SENSE^-$, which are the positive and negative voltage inputs across the sensing resistor $R417 = 25 \text{ m}\Omega$. It records the integral of the flowing current to get the charge count.

The gas gauge monitors the available battery capacity. The zeroing function of the counter behaves as follows. First, the state of charge is saved in the status register. Then, when the battery is fully charged, it receives a '0', while when it gets discharged, it is subtracted. The goal is to save the total battery charge level in the register. The operation is programmed in the control register.

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The ADC included in the *LTC2942* can be used both to measure the battery voltage on $SENSE^-$ and the temperature through an on-chip temperature sensor. The \overline{AL}/CC is a dual function pin for Alert Output and Charge Complete Input. It is connected to the microprocessor with the *-PWR_IRQ* signal.

The *LTC2942* is a slave-only device. It supports the I^2C standard and the communication with the master bus is achieved through a 2-wire interface.

Voltage Level Translator

The SCL (input only) and the SDA (bidirectional) signals of the battery gas gauge are connected to the SCL_B and SDA_B of the Voltage Level Translator. Labelled as 1404, it is an NXP Semiconductors[®] PCA9517ATP. The peripheral for the connection with the microprocessor is the $I^2C(1)$.

Battery Charger

The battery charger, labelled I403, is an *Analog Devices*[™] *LT3650*. It is a high voltage battery charger whose charging algorithm is described below.

Start-up: The nominal input voltage of the LT3650 is V_{in} =24 V, with a range of 9-32 V. The *BOOST* pin works as a supplier and drives the internal switch. It is connected to an internal capacitor C412, whose charging starts, when V_{in} is 3 V above the SW pin.

Output decoupling: The BAT pin is connected to the ground with two bypass capacitors in parallel: $C410=10 \ \mu\text{F}$ and $C411=100 \ \mu\text{F}$. It is also connected to the $Q402 \ \text{PMOS}$ transistor, which serves as a protection device to prevent damages in case of inversion of the battery.

Charge current programming: The charge current is programmable up to 2A using a resistor, currently selected as $R420=20 \text{ k}\Omega$. The current sensing resistor is $R_{SENSE}=0.05 \Omega$. The inductor $L401=6.8 \mu$ H sets the amount of ripple current. CHRG and FAULT are two status pins, which indicate the charge status output and the fault status output. The connection to the microprocessor is provided through the signals PWR_CHRG and PWR-FAULT.

Timer termination: The device provides an internal timer. The TIMER pin is connected to a C_{TIMER} =68 nF capacitor. It is used to program the end-of-cycle, with t_{EOC} ~3 h. The precondition limit time, when the bad-battery fault is generated, is given by t_{PRE} ~22.4 min. t_{PRE} ~22.4 min.

Preconditioning: The battery operating voltage range is V_{BAT} =3.0-4.2 V. The output voltage is sensed through the BAT pin. If the voltage on this pin is below V_{BAT} , the battery charger works in precondition mode, in which the current limit is 15% of the maximum available current.

The charging terminates when the current falls to 1/10 of the maximum current.

The battery connector, labelled J400, is a *Hirose Electric Group® DFC9*.

Boost Converter and Step-Down Converter

The boost converter, labelled *I400*, is a *Texas Instruments*[™] *LM2733*. It is a high-frequency switching regulator operating at 1.6 MHz through the current mode control.

The step-down converter, labelled *I401*, is a *Texas Instruments*^m *TPS82130*. It is based on Direct Control with two operating modes: pulse width modulation (PWM), with a switching frequency of 2 MHz, and power save mode (PSM), with a quiescent current range of 20-35 μ A.

3.1.6 Mechanical design

The MSP board mechanical design consists of an enclosure to accommodate the footprint of 100 mm x 100 mm of the PCB and a lateral panel board with a form factor of 50 mm.

The enclosure consists of black ionized aluminum for the body, and a technical plastic with a sealing gasket for the upper part.

The main elements of the MSP board are arranged as follows:

- The rechargeable Li-Ion battery, whose dimension is 90 mm x 60 mm, is placed in the lower part of the board.
- Since one of the internal sensors is an accelerometer, whose role is to measure possible vibrations of the board, it is necessary to firmly support it without distorting the vibration propagation or creating resonances.
- The antenna for the radio module is internal, flat, and adhesive, attached to the plastic panel.
- The connectors for the development and debug part are hidden internally in the final assembly.
- Three circular connectors are provided for the sensors.
- Another circular connector is provided for the ancillary communication module.
- Body-integrated holes are present for fixing the enclosure to the workpiece or machine.

Figure 24 to Figure 26 show the rendering of the 5G-SMART enclosure.

Figure 24 5G-SMART MSP enclosure rendering

Figure 25 5G-SMART MSP connectors

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Figure 26 5G-SMART MSP inner enclosure rendering

3.2 Software Architecture

The software architecture of the MSP is shown below in Figure 27.

Figure 27 MSP Software Main Architecture

The core of the sensor platform is the STM32F4 series microcontroller. After powering up the platform, the controller first initializes the system with the corresponding system and peripheral clocks and the system interrupts. The controller is programmed to operate at 168 MHz generated by the internal PLL clock. It also generates 48 MHz for USB and a 25 MHz clock for the Ethernet PHY chip.

The Peripherals of the microcontroller SPI, I2C, UART ports, Ethernet PHY GPIO and their corresponding DMA channels are initialized. After successful initialization, the LwIP TCP/IP stack is initialized, network connection with the 5G module via the Ethernet/USB ports initialized, and IP address via the DHCP received.

After successful DHCP acknowledgment, the controller opens the socket communication. It opens two ports, one for UDP Data transmission and the other for receiving the reconfiguration over the LWM2M protocol. UDP is used for transmission as it has low overhead and efficiency compared to other protocols. LWM2M is used for remote reconfiguration of sensor platform parameters.

Furthermore, the controller creates two COM ports on UART, one to communicate with the SARA-R5 module via the AT Commands and the other for debugging purposes.

To guarantee a concurrency of the applications, a real-time operating system is integrated that manages all functionalities as tasks despite multiple sensors and network interfaces.

For the MSP, a FreeRTOS solution (open source) is integrated. The following tasks are created:

- Tasks for sensor interfaces (external and internal).
- UDP server task for data packet generation and transmission.
- Reconfiguration task hosted as an LWM2M Server.

3.2.1 On-board Sensor Task

The on-board gyroscope and humidity sensor are interfaced to the controller via the I2C interface. These sensors are used for internal diagnostic purposes regarding the housing temperature, orientation, and water intrusion. Hence, the task (Figure 28) is set to a low priority level, with the task triggered by a timer every 2-3 seconds.

Figure 28 SW architecture for on-board sensor

On the timer trigger, the controller initiates a data transfer by placing the register address that contains the data on the I2C interface and sending it to the sensor module.

3.2.2 External Sensors

While the AE sensor system is based on piezo technology and makes use of the IEPE standard, the MSP has to be able to integrate external sensors operating on multiple sensor principles for which IEPE does not apply. The external sensors are connected to the microcontroller via the SPI interface, which offers enough flexibility and modularity. The controller acts as a master device and sets up the sensor modules as dependent devices with their respective configurations. Each SPI interface has a Direct Memory Access (DMA) to enable CPU offloading. This setup allows the sensors to write directly the data from their module to the controller's memory. Once a transfer is done (depending on the configuration), an interrupt is generated, allowing the controller to access and pre-process the data,

followed by packing and sending it as UDP packets. The data flow architecture is illustrated in Figure 29.

Figure 29 External sensor SW architecture

In the RTOS configuration, the corresponding tasks of the sensor are in a sleep state until the interrupt from the DMA channel is received. After reception of interrupt, the task quickly processes and packs the data as UDP and sends it to the UDP TX thread.

Before sending the data, the corresponding task requests the SARA-R5 module for the timestamp by triggering an interrupt to the module. This timestamp is received on the UART pins. The controller receives the stream in a buffer, which is then retrieved by the corresponding task which triggered the interrupt. After appending the data buffers and the time stamp, the stack then passes the data on to the UDP TX thread to send it to the destination.

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3.2.3 Reconfiguration

The MSP provides additional flexibility to enable reconfiguration of specific platform and sensor related parameters dynamically during the process. Therefore, the LWM2M protocol runs on top of the UDP stack to ensure easy remote configuration of the sensor platform from, e.g., the factory cloud. The microcontroller establishes the LWM2M server on one of the ports to receive the configuration commands from the remote client. Figure 30 shows the corresponding data flow.

Figure 30 Reconfiguration server SW architecture

The server receives the configuration request on the port and validates if it is applicable for its sensor type or platform configuration. If the configuration is valid, then the configuration is sent to the corresponding sensor interface via the SPI to reconfigure the sensor module. After successful configuration, it sends a positive acknowledgment to the client.

Since the MSP supports various sensors and each sensor has its specific configuration, the possible configurations are listed below.

1	Mainboard	Enable/ Disable sensor • Disable specific on-board/external sensor when not needed.
		 IP configuration: Destination IP address/port modification Send to redundant destination IP address Modify board IP address (static/DHCP)
		Prioritization of sensor
		Raw or processed data (FFT/FFT length, wavelet transform, peak detection, dynamic resolution of data)
		Request for configuration details
		Parsing sub configuration of sensors directly to sensors via SPI
2	Vibration sensor/ microphone	Sampling Frequency • Set value, increase or decrease
		Optional parameters for the sensors (integrated FFT, smoothing, filtering)
		Sensitivity modification
3	Strain gauge/Torque/Force	Sampling frequency
	sensor	Sensitivity configuration
		Calibration request and value
4	Temperature	Sampling frequency
5	SARA RE modulo	Calibration request
5	SARA-RS IIIOUUIE	CellTime [™] parameter configuration
6	Internal Sensor	Threshold for triggering an alarm Sampling frequency

Table 2 MSP configuration options

3.2.4 Implementation of signal processing

In order to extend further the platform's versatility, the microcontroller is well capable of doing onboard signal processing. The raw data from the sensor modules is transformed to processed values by translation from indirect to direct measurands (for temperature, strain sensors), e.g. with a calibration table. The controller can also perform advanced signal processing such as Fourier Transform and digital filters (e.g. Kalman) and send the processed data to the end application.

This processing can be controlled and configured remotely, depending on the application needs, via the reconfiguration of the LWM2M server.

3.3 Synchronization of data sources

3.3.1 Description of synchronization architecture (CellTime[™])

The CellTime[™] feature is split between the SARA-R5 modem and a dedicated service (Figure 31). Using three AT commands, the modem permits the feature in a specific operation mode (PPS or timestamp of external interrupts) and to read and set relevant time information.

The service has the following responsibilities and features:

- manage a registry of groups of modules
- ensure the synchronization of groups of modules
- propagate UTC time from modules with GNSS visibility to others in the same group

Synchronization of groups of modules can happen only when connected to the same LTE (LTE-M/NB-IoT) base station. Modules can join or exit the group at any time, and the service will take care of sending appropriate commands to align their local time reference with that of the devices already in the group. If any device belonging to the group can get a GNSS fix, the service will adjust the local time scale of the group to UTC, even for devices that are deep indoor.

The service provides two endpoints. Customers manage and register their modules using the REST endpoint, while modules use the MQTT endpoint for updating their status and receive synchronization-related commands.

Figure 31 High-level diagram of the interactions for time synchronization

3.3.2 Implementation of time sync in the MSP

The MSP is linked with the SARA-R5 module via the UART interface. The MSP creates a virtual COM port to have a duplex communication. Before receiving the timestamp, the MSP first sets up the SARA-R5 module at the system initialization phase. It sends the AT commands to connect to the base station, register the device, and enable the CellTime[™] functionality. Then, the trigger for the timestamp is set up by configuring the GPIO of the SARA-R5 module using AT commands. With this, the MSP is ready to receive the timestamp. Various tasks, which require timestamps, trigger an interrupt, upon which a timestamp is requested by the SARA-R5 module and sent to the MSP via the UART interface. The ISR

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of the MSP has a state machine that converts the timestamp data, removes the headers, and then saves it to the buffer attached to the data packet for transmission.

3.3.3 Implementation of stand-alone time sync module

Some applications require an accurate timestamp for synchronization of wired and wireless data sources. One example is the extraction of machine positions or feed rate generated from the integrated industrial PC of a machine. Typically, a standard interface such as Ethernet is present only and no GPIO. To nevertheless enable synchronization for data fusion, a Raspberry Pi-based SARA solution was developed. The Raspberry Pi acts as a bridge and hosts a Network Time Protocol/ Precision Time Protocol (NTP/PTP) server through which the PC can request timestamp information. The NTP/PTP server fetches the reference time from the SARA-R5 module. Due to the flexibility and a unique interface, this stand-alone solution can be easily interfaced to any machine/PC to receive accurate time data from the base station.

In addition, this device also has an important feature to synchronize the timestamps to UTC time. Typically, the timestamp generated has a reference time that is different from the current time (UTC time). Hence, to convert it to UTC time, the module first receives the reference time from GNSS, which is in UTC, and propagates that information to the base station service via MQTT protocol. The CellTime[™] service on the base station configures and then synchronizes all its devices to receive the timestamp corrected to UTC time.

4 Implementation of versatile sensor data processing pipeline

4.1 Setting up the application/execution/runtime environment

The data processing pipeline is deployed on the virtualized infrastructure provided by German Edge Cloud¹ (GEC), integrated into the Fraunhofer IPT network (chapter 4.2.3). Four VMs are utilized in the GEC OpenStack space with static IP addresses assigned to them, accessible across VPN connections to Fraunhofer IT, and are routable to and from both the sensor boards over the 5G radio network as well as the wired networking towards the machining equipment.

Ubuntu Linux server distributions are installed on three of the VMs, and a Kubernetes² cluster is deployed for the fully cloud-native, containerized components of the software pipeline. Kubernetes is chosen as the de facto industry standard of container orchestration system, for which the most versatile reusable components and know-how are available.

Furthermore, a single VM is installed with the pre-existing QNX-based process monitoring software named *GEM-VM* from Marposs. The interconnection of components concerning the cloud deployment is shown in Figure 32. Solid lines show the *data path* of raw and pre-processed sensor measurements, and dashed lines indicate the direction of control messages. Dotted functions are internal to and only accessible by other functions inside the Kubernetes cluster.

Figure 32 Functions in the Kubernetes cluster

Kubernetes is installed with *Kubespray* following the quick start guide at <u>https://kubespray.io</u>. This will set up a full container orchestration system with the Calico networking plugin and an internal DNS service. The latter will be used for name-based service discovery of the various components of our software pipeline. A single element of customization of Kubespray is needed: the static IP addresses

¹ <u>https://www.friedhelm-loh-group.com/en/unternehmensgruppe/gec.asp</u>

² <u>https://kubernetes.io/</u>

of our three VMs have to be entered in the <code>hosts.yaml</code> file as an <code>ansible_host</code> field for each server:

```
all:
   hosts:
    srv1:
      ansible_host: XXX
   srv2:
      ansible_host: XXX
   srv3:
      ansible_host: XXX
```

After the execution of the Ansible playbook, a shared Kubernetes *secret* is added to the installation for allowing access to the Fraunhofer GitLab Docker image repository used for both development and distribution of container images:

```
$ docker login registry.gitlab.cc-asp.fraunhofer.de:4567
Username: ...
Password: ...
$ kubectl create secret generic vfk \
        --from-file=.dockerconfigjson=/home/ubuntu/.docker/config.json \
        --type=kubernetes.io/dockerconfigjson
secret/vfk created
```


Figure 33 Screenshot of GEM-Visu

With this, the infrastructure is ready to handle Kubernetes control commands using the standard kubectl command-line tool, or optionally the *Kubernetes Dashboard* module, which is planned to be enabled for the validation and demonstration phases of the project.

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Monitoring the state of the sensor control loop is done using the graphical visualization tool *GEM-Visu* by Marposs (see Figure 33). The machine data (first plot) and signal levels for the different sensors (second plot) detected by the *GEM-VM* module can be visualized.

It is possible to integrate the Web GUI into *GEM-Visu* as a plugin. This option will be evaluated during the project validation phase.

4.2 Implementation of sensor data processing pipeline

The implementation of the sensor data processing pipeline closely follows the described architecture in deliverable D3.2 [5GS20-D320]. All services defined there were implemented separately and are to be integrated into a single system. For the integration and interoperability of these services, additional functionalities described in the following paragraphs are needed and developed.

4.2.1 Reliability features

To ensure continuous functionality and increase the reliability of the critical data paths, the ability for multiple deployments of the sensor processing service was implemented. For testing the deployment, the first two instances of sensor processing are called and running in parallel. These instances are getting the same data from the same sensor, so if one of the instances crashes, the other will still be running. Therefore, the sensor needs to send the same data twice but to different instances of the service. The orchestration of these services is done by Kubernetes, as described in section 4.1.

4.2.2 Predefined procedures and routing rules

To implement the behavior of the cloud system, we need predefined procedures and rules for the routing of messages exchanged between the services. The services described in deliverable D3.2 will be extended with complementary modules to describe these routing functionalities in a sequence diagram. The data processing service, the sensor configuration service, and the *GEM-VM* service are described in deliverable D3.2 and remain unchanged. For the data storage service, the object storage from Kubernetes is suited to be the database, which is a replicated document storage that already, moreover, provides capabilities to register for content changes conveniently. The Kubernetes operator was not described before as a service, but it plays a significant role in the orchestration of the pre-processing service. The GEM GUI service will now be called Web-GUI (Figure 32). This service will be used as GUI to monitor the *GEM-VM* and the configuration of sensors, as well as interaction of the user with all the sensor processing pipeline services. It is planned to include the GEM-GUI as a plugin into this web GUI. As a potential end-user, a machine technician is considered for the interaction with the Web-GUI.

In this context, four main use cases are defined:

- Connect
- Reconfigure
- Unplug
- Failover

Connect

The Connect case handles the plugging of a sensor into the system by the (end-)user (**Error! Reference source not found.**). After the physical connection and the sensor are booted up, the MSP sends an

initial connection message to the sensor configuration service. The connection between the MSP and the sensor configuration service is established via the LWM2M protocol. It is mainly used to exchange configuration information between the two modules. The sensor configuration service also includes a REST API to exchange messages between the Kubernetes operator and the data processing service. After receiving the connection of a new sensor, this information is forwarded to the Kubernetes operator. The user now must confirm that a new sensor has been plugged in and specifies the associated machine of the connected sensor. The Kubernetes operator then starts a new instance of the data processing service.

Figure 34 Predefined procedure – Connect

The IP and port address of this new instance will be forwarded to the sensor configuration service, thus configuring the respective sensor with the destination IP and port address. After the sensor configuration, the configuration information is sent to the sensor processing service, and the sensor

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is triggered to send data. The configuration information is used to compare the configuration of the sensor from which the data is received. If the configuration is the same, the data will be processed and forwarded to the *GEM-VM*. Otherwise, a signal is sent to the sensor to stop the data transmission, and the sensor configuration service will start again with the configuration procedure. The underlying commands of the described procedure are contained in Figure 34.

Reconfigure

The reconfiguration of a sensor during runtime represents a widespread case. Here, a user can set a new configuration for the sensor via the Web-GUI service (Figure 35). The Web-GUI service has a connection through a REST API call to the sensor configuration service and can forward the new configuration of the sensor. The sensor configuration module will stop the sensor's data transmission, and the new configuration is sent to the sensor. At the same time, this configuration is sent to the data processing service, and the procedure described in the Connect case takes place.

Figure 35 Predefined procedure – Reconfigure

Unplug

The scenario for unplugging the sensor is designed to change sensors between different processes or during maintenance. The sensor configuration service recognizes the unplugging of the sensor by the user (Figure 36). The alert of losing connection to the sensor is sent to the Web-GUI and must be approved by the user. After that, the Kubernetes orchestration instance will be informed to shut down the data processing service for this sensor. After closing the processing service instance, the sensor configuration service will receive confirmation.

Figure 36 Predefined procedure – Unplug

Failover

The failover case describes the failure of an instance of the data processing service. The Kubernetes operator realizes this failure and immediately starts a new instance (Figure 37). After that, the new IP and port address of this instance will be received. The following part of the overall procedure is the same as in the reconfiguration case. The sensor will be configured again with the new IP and port address related to the new data processing instance.

Figure 37 Predefined procedure – Failover

4.2.3 Integration of factory cloud platform with 5G network and industrial LAN

The 5G network and the machine network at Fraunhofer IPT had to be integrated with the factory cloud solution on-premise. The factory cloud can ensure interaction between different sensors and actors (i.e., machines and devices) and be a scalable connectivity solution for the manufacturing environment. The biggest challenge is to realize the different levels of access needed, maintaining data security, and the dynamic data exchange between the different integrated networks. In order to meet these challenges, an integration concept for the factory cloud was developed.

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Figure 38 Zones inside the factory cloud at Fraunhofer IPT

The factory cloud is split into Private Zone, Shared Zone, and Public Zone (Figure 38). These zones are separated from each other and have individually assigned access parameters and responsibilities. The Private Zone is only accessible for internal users of Fraunhofer IPT and offers access to the shopfloor, cloud systems, and the office network. Within the Shared Zone, project partners can also be added and have access to test networks and cloud systems. Finally, the Public Zone can be considered a remote cloud environment which external users can access.

Figure 39 Defined access rules of different networks at Fraunhofer IPT

Error! Reference source not found. shows the currently defined access rules between the different networks, like the shopfloor, office, 5G, and cloud network. At the current state, bi-directional access to the cloud system, to the office and shopfloor network is denied. Due to the prototypical state of the cloud system, this is implemented to avoid security and safety issues. Only one-way communication from the office and shopfloor networks and access from external users to the factory

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cloud are allowed. The access rules for the 5G core to the cloud system and other networks like other factories or the public 5G network, are not defined. The access rules for the zones of the cloud system are defined so that the Private Zone has access to the other zones and the Shared Zone has access to the Public Zone, but without any communication the other way.

4.2.4 Virtualization of data processing

Genior Modular (GEM) is an autonomous, intelligent tool and process monitoring system providing an automatic real-time representation of a current production process. Safe and reliable metal cutting processes are essential for economically efficient production. *Genior Modular's* multi-criteria monitoring strategy adapts automatically to machining processes. This means, that the system records all relevant signals and sets the limits based on special algorithms. During the following cutting cycles, *Genior Modular* adjusts the limits automatically. Experts can change and manually set the limits.

In a standard installation, the monitoring software runs on the CPU unit - a small embedded PC for installation in the control cabinet. The operating system used on this unit is QNX to fulfill hard real-time requirements. Typically, the CPU unit is connected to the computer numerical control (CNC) via a fieldbus technology, such as Profibus or Profinet, to receive all relevant data from the CNC. If required, further sensor modules can be connected via CAN-Bus and mounted on a DIN rail

In the context of the 5G-SMART project, the *Genior Modular* monitoring software is ported to the factory cloud of Fraunhofer IPT. This is possible since QNX is also available for the x86 CPU architecture. The main difference between the virtualized and the physical *Genior Modular* is the lack of hardware like CAN-Bus or Profinet. This restriction makes Ethernet the only access to the outer world. To avoid developing a custom version of *Genior Modular* for the 5G-SMART project, a data receiver was created, pretending to be a CAN-Module using the corresponding driver interface. In this way, future updates of Genior Modular can be easily adapted to the cloud solution.

Improvement of the resilience of the data transmission via 5G is achieved by transmitting the sensor data on multiple channels. Each data packet contains a timestamp so that the most recent value is known, and obsolete values can be omitted. The software that performs the timestamp check is the receiver, as mentioned earlier.

4.2.5 Implementation of interfaces and protocols for M2M communication between machine PLC and virtual machine in the factory cloud

The last component in the feedback control chain is the gateway to the machine to actively influence the real machine during process runtime. Since the beginning of the project, attempts were made to find a date for installing this gateway in the form of the *Genior Modular CPU* unit via Profinet. Unfortunately, due to various confidentiality declarations required by the machine tool manufacturer for the installation and the Covid-19 pandemic, an installation could not be carried out to date despite all efforts. Since it is not yet foreseeable if and when an installation together with the machine tool manufacturer will be possible, an industrial Raspberry Pi will be connected to the machine via Ethernet as an alternative solution for the time being. The protocol between the monitoring in the cloud and the CPU unit at the machine is the very efficient binary protocol used for Profibus.

5 Conclusion and outlook

After describing the design options for the two sensor solutions and the sensor data processing pipeline in 5G-SMART deliverable D3.2, the most appropriate options were selected and implemented, with the goal of fulfilling the requirements of the different use cases on one hand and achieving a sustainable solution on the other hand.

A sustainable solution in this context means that industrial requirements regarding mechanical robustness were taken into account. Furthermore, flexibility was achieved by a modular approach allowing to connect different sensors on one hand, and on the other hand by integrating different communication interfaces like USB and/or Ethernet to use of different 5G communication devices becoming available.

Two sensor systems have been successfully developed: a versatile multi-sensor platform that is feature-rich and provides vast configurability and modularity, and an acoustic emission sensor system with powerful hardware and integrated computing capacity. For the first time, 5G devices have been developed, that go beyond providing connectivity and can be directly applied to solve challenges in today's production. The deliverable provides detailed information about electronic design, embedded software development as well as the integration of 5G communication capabilities and can serve as a blueprint for future 5G-based products.

For the processing of the sensor data, a modern factory cloud has been set up based on OpenStack and Kubernetes, reflecting the most up-to-date platforms. Furthermore, partners in 5G-SMART have provided novelties to integrate the factory cloud into the Fraunhofer IPT office network, shopfloor IT, and the 5G network. Additionally, an innovative concept with security zones has been developed to serve the connectivity and computation needs in today's networked production on one hand, but on the other hand also taking security concerns of manufacturing companies into account. Finally, for the versatile processing of sensor data and orchestrated interaction of factory cloud and wireless sensor systems, a novel processing environment with services running on virtual machines has been realized. Thus, the concepts for the data processing pipeline developed in 5G-SMART may serve as a blueprint for future 5G-enabled smart manufacturing.

In the remaining time of the project, the implemented solutions, both sensor systems and the data processing pipeline, will be used to validate 5G for the use cases in relevant manufacturing tasks, reflecting real-world problems in today's production. The multi-sensor platform will be used for monitoring the milling process of a turbine component, while the established factory cloud will be used for processing of the transmitted sensor data and feedback to the milling machine. Furthermore, the machining of a structural part will be monitored with the multi-sensor platform equipped with strain gauges to measure mechanical strain during machining process. The acoustic emission sensor system will be used to detect material contact and tool breakage. All planned applications serve for the validation of the use cases and their contribution to smart manufacturing with respect to quality, sustainability, flexibility, utilization and productivity. The results of the evaluations will be made available in the deliverable D3.4 towards the end of the project.

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